

Claim Amendments

Claim 1 (currently amended). A method for fabricating a double gate MOSFET, which comprises the steps of in the following sequence:

providing a substrate structure having a silicon substrate layer, a first insulation layer disposed on the silicon substrate layer, a first spacer layer disposed on the first insulation layer, and a semiconductor layer disposed on the first spacer layer;

B1 patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET;

depositing a second spacer layer on the semiconductor layer structure and the first spacer layer;

completely embedding the semiconductor layer structure in the first and second spacer layers by patterning the first and second spacer layers;

depositing a second insulation layer on a structure formed of the first and second spacer layers;

vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case;

filling the depressions with an electrically conductive material;

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forming a contact hole in the second insulation layer;

selectively removing the first and second spacer layers through the contact hole made in the second insulation layer;

applying third insulation layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; and

introducing a further electrically conductive material into the region of the removed spacer layers.

Claim 2 (original). The method according to claim 1, which comprises forming the substrate structure by applying the

first insulation layer, the first spacer layer, and the semiconductor layer one after another.

Claim 3 (original). The method according to claim 2, which comprises recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

Claim 4 (original). The method according to claim 1, which comprises

forming the substrate structure by the steps of:

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providing the silicon substrate functioning as a first semiconductor substrate;

applying the first insulation layer on the first semiconductor substrate;

providing a second semiconductor substrate;

applying the first spacer layer on the second semiconductor substrate;

connecting the first and second semiconductor substrates to one another using a wafer bonding process between the insulation layer and the first spacer layer; and

reducing a thickness of the second semiconductor substrate resulting in the semiconductor layer.

Claim 5 (original). The method according to claim 1, which comprises forming the first and second spacer layers from silicon nitride.

Claim 6 (original). The method according to claim 1, which comprises planarizing the second insulation layer after being deposited.

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Claim 7 (original). The method according to claim 1, which comprises carrying out the step of selectively removing the first and second spacer layers through the contact hole made in the second insulation layer.

Claim 8 (original). The method according to claim 1, which comprises forming the electrically conductive material from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide.

Claim 9 (original). The method according to claim 8, which comprises forming the doped polycrystalline silicon by chemical vapor phase deposition and a doping is performed during the deposition.

Claim 10 (previously amended). The method according to claim 1, which comprises selectively removing the first and second spacer layers by wet-chemical etching.

Claim 11 (original). The method according to claim 1, which comprises applying the third insulation layers using a thermal oxidation process.

Claim 12 (original). The method according to claim 11, which comprises producing a relatively thin oxide layer on the surface of the semiconductor layer structure and producing a relatively thick oxide layer on the inner walls of the region of the removed spacer layers.

Claim 13 (original). The method according to claim 1, which comprises forming the further electrically conductive material from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide.

Claim 14 (original). The method according to claim 13, which comprises forming the doped polycrystalline silicon by chemical vapor phase deposition and a doping is performed during the chemical vapor phase deposition.

Claim 15 (original). The method according to claim 1, which comprises applying an oxide layer as the first insulation layer.

Claim 16 (original). The method according to claim 1, which comprises applying a silicon layer as the semiconductor layer.

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Claim 17 (original). The method according to claim 1, which comprises depositing an oxide layer as the second insulation layer.

cont.

Claim 18 (original). The method according to claim 1, which comprises applying oxide layers as the third insulation layers.

Claim 19 (original). The method according to claim 9, which comprises using arsenic atoms in the doping process.

Claim 20 (original). The method according to claim 14, which comprises using phosphorous atoms in the doping process.

Claims 21-25 (canceled).
